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USB-61210

4-CH 16-Bit 2MS/s Simultaneous-Sampling USB DAQ Module

User's Manual

Manual Rev.: 1.00

Revision Date: July 31, 2017

Advance Technologies; Automate the World.

Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

Additional information, aids, and tips that help users perform tasks.

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The USB-61210 is a 16-bit high-speed USB 2.0-based DAQ module equipped with 4 analog input channels providing simultaneous sampling at up to 2MS/s per channel. The USB-61210 delivers high accuracy and excellent dynamic performance at maximum sampling rates and features flexible trigger function. In addition, onboard 256MS FIFO ensures no data loss during acquisition even with heavy loading on CPU or system.

The USB-61210 is USB bus powered and equipped with removable screw-down terminals for easy device connectivity, and the included multi-functional stand can be used for desktop, rail, or wall mounting.

Suitable for high-speed data acquisition, laboratory and medical research, the USB-61210 provides a reliable measurement solution at an affordable price.

1.2 Features

- Hi-Speed USB 2.0
- USB bus power
- 4-CH simultaneous-sampling analog input, up to 2MS/s per channel
- Analog and digital triggering
- 500VDC bus isolation
- Removable screw terminal
- Lockable USB cable for secure connectivity
- Ready-to-use testing application (U-Test) included

1.3 Applications

- Automotive testing
- High-speed data acquisition
- Laboratory research
- Medical
- I/O control

1.4 Specifications

1.4.1 General Specifications

Digital I/O Specifications	
Number of channels	8-CH programmable function digital input (DI) 4-CH programmable function digital output (DO)
Compatibility	LVTTL (single-end) (supports 3.3V and 5 V DI but 3.3V DO)
Input voltage	Logic low: VIL = 0.8 V max; IIL = 0.2 mA max.Logic high: VIH = 2.0 V min.; IIH = 0.2 mA max.
Output voltage	Logic low: VOL = 0.5 V max; IOL = 10 mA max. Logic high: VOH = 2.6V min.; IIH = 10 mA max.
Supporting modes (only one can be selected and function at the same time, please see Section 3.1.5: Programmable Function I/O)	8-CH LVTTL DI and 4-CH LVTTL DO 2-CH 32-bit general-purpose timer/counters: Clock source: internal or external Max source frequency: internal: 80 MHz; external: 10 MHz 2-CH PWM outputs": Duty cycle:1-99% (please see Section : Mode 10: PWM Output) Modulation frequency: 20 MHz to 0.005Hz
Data transfers	Programmed I/O

Physical, Power, and Operating Environment	
Interface	High speed USB 2.0 compatible, mini-USB connector
Dimensions	156 (L) x 114 (W) x 41 (H) mm (6.14 X 4.49 X 1.61 in.)
I/O Connector	Two 20-pin removable screw-down terminals
Power requirement	USB power (5 V @ 500 mA)
Operating environment	**Ambient temperature:** 0 to 55°C **Relative humidity:** 10% to 90%, non-condensing
Storage environment	**Ambient temperature:** -20 to 70 °C **Relative humidity:** 5% to 95%, non-condensing

1.4.2 Analog Input

Resolution	16 bit
Channels	4 differential (simultaneous sampling)
Maximum sampling rate	2MS/s per channel
Programmable gain	1, 5
Input range (voltage)	± 10 V, ± 2 V
Offset error	± 1mV (gain=1) ± 0.2mV (gain=5)
Gain error	Typical: ± 0.01% of FSR (gain=1 & 5) Maximum: ± 0.02% of FSR (gain=1 & 5)
-3dB bandwidth	630kHz (gain=1) 600kHz (gain=5)
CMRR (fin=1 kHz)	80 dB (gain=1) 90 dB (gain=5)
SFDR (fin=10 kHz)	108 dB (gain=5)
SINAD (fin=10 kHz)	89 dB (gain=1 & 5)
THD (fin=10 kHz)	100 dB (gain=1 & 5)
SNR (fin=10 kHz)	89 dB (gain=1 & 5)
ENOB (fin=10 kHz)	14.3-Bit (gain=1 & 5)
Temperature Drift: Gain Error	5 ppm/°C (gain=1 & 5)
Temperature Drift: Offset Error	50µV/°C (gain=1) 20µV/°C(gain=5)
FIFO buffer	256 Msamples
Trigger sources	Software, external digital, analog trigger (from one analog input channel)
Trigger mode	Post trigger, pre-trigger, delay trigger, middle trigger, gate trigger, post or delay trigger with re-trigger
External A/D conversion source	Yes (from CONV)
Input coupling	DC
Overvoltage protection	Power on: ± 35 V Power off: ± 15V
Input impedance	1 GΩ

Data transfer	Programmed I/O, continuous (USB bulk transfer mode)

1.5 Schematics

NOTE: All units are in millimeters (mm)

1.5.1 Module

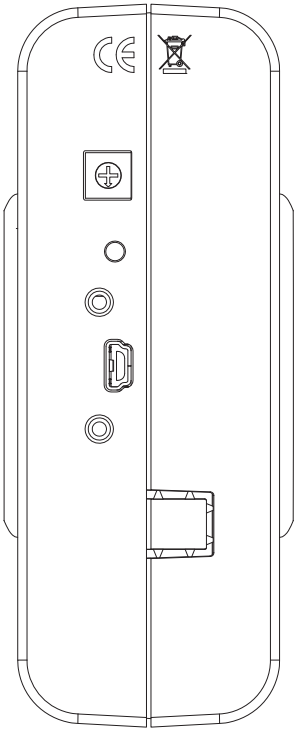

Figure 1-1: USB-61210 Module Rear View

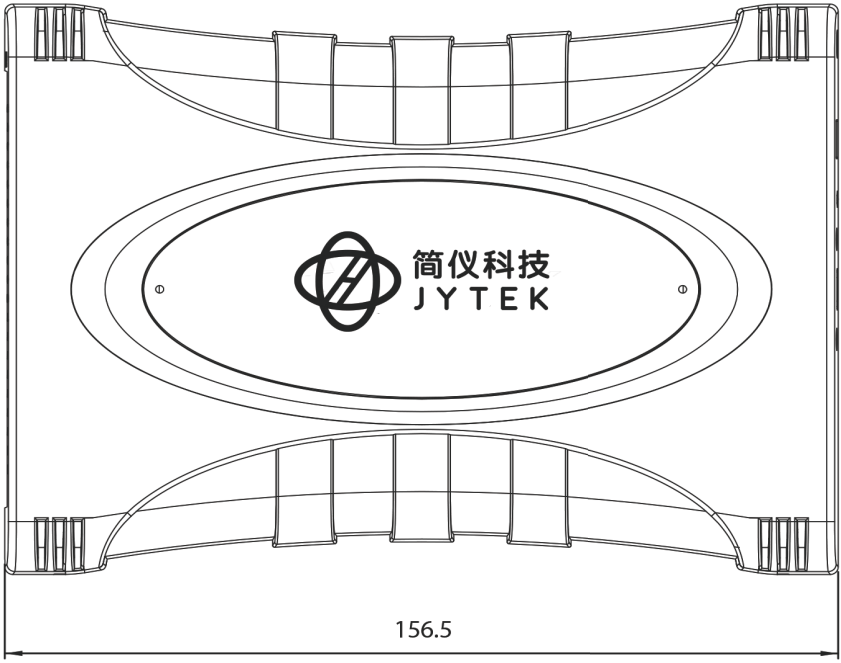

Figure 1-2: USB-61210 Module Side View

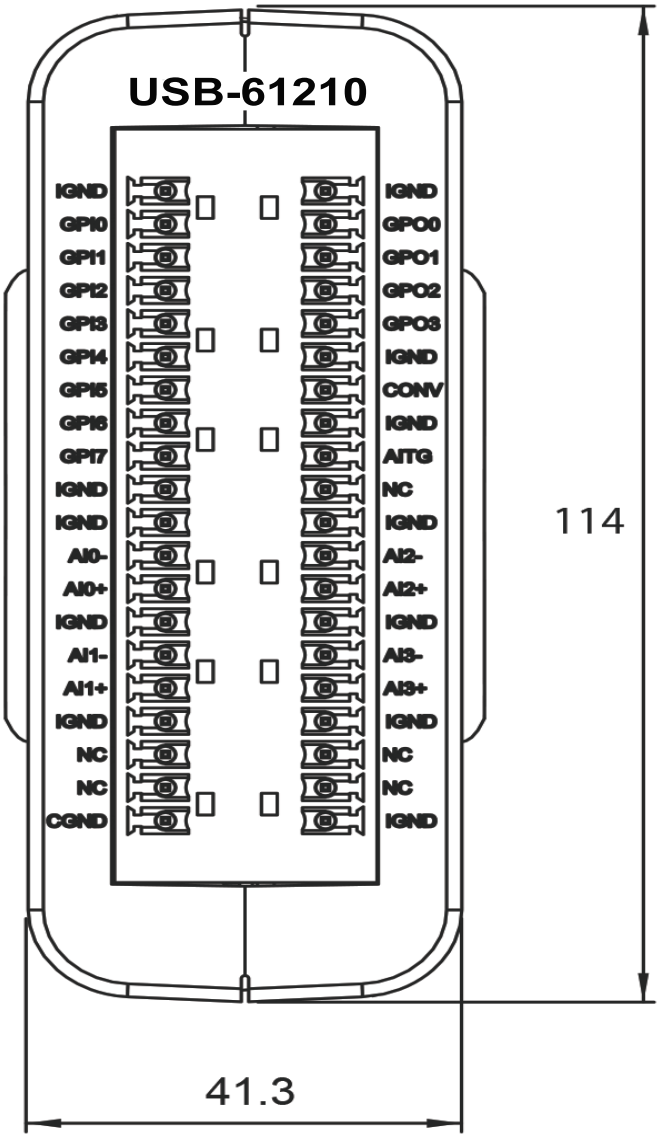

Figure 1-3: USB-61210 Module Front View

1.5.2 Module Stand

The multi-function USB-61210 stand is compatible with desk, rail, or wall mounting. To fix the module in the stand, slide the module body into the stand until a click is heard. To remove the module from the stand, twist the bottom of the stand in a back-and forth motion and separate from the module.

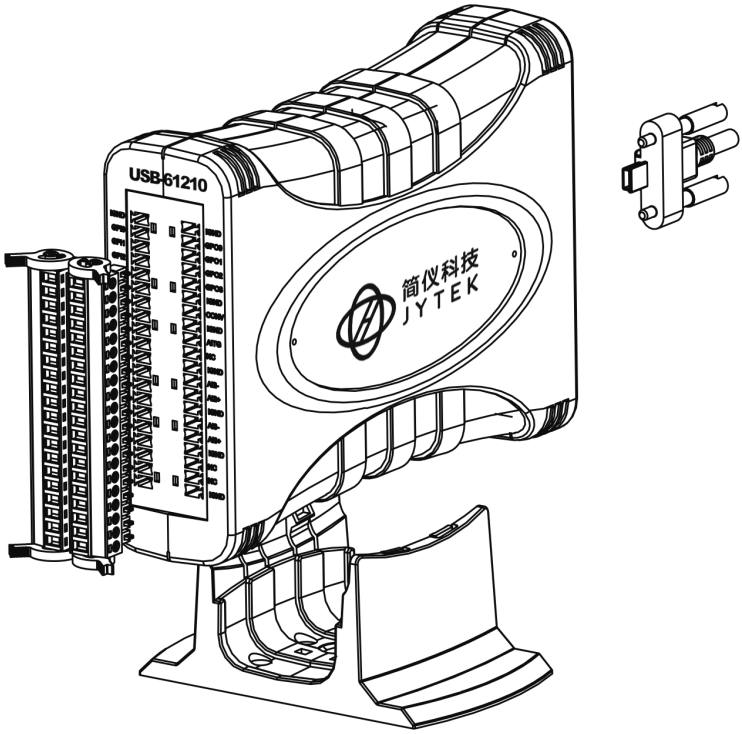

Figure 1-4: Module, Stand, Connector, and USB Cable

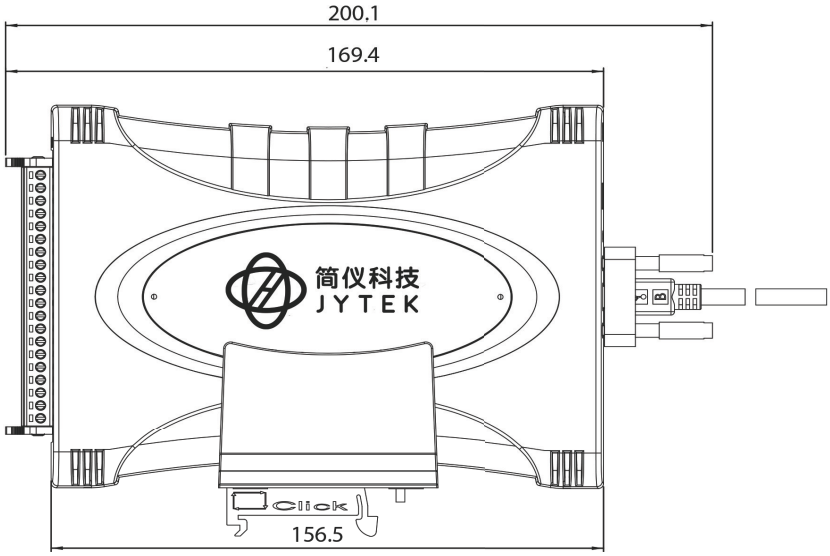

Figure 1-5: Module, Stand, & Wall Mount Kit Side View (w/ connections)

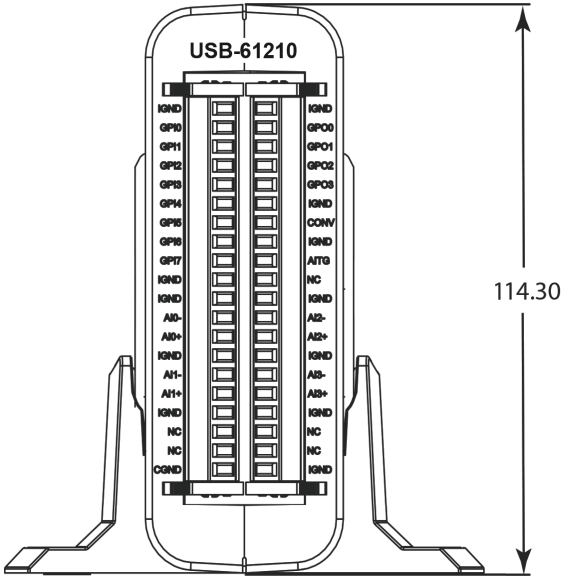

Figure 1-6: Module in Stand Front View

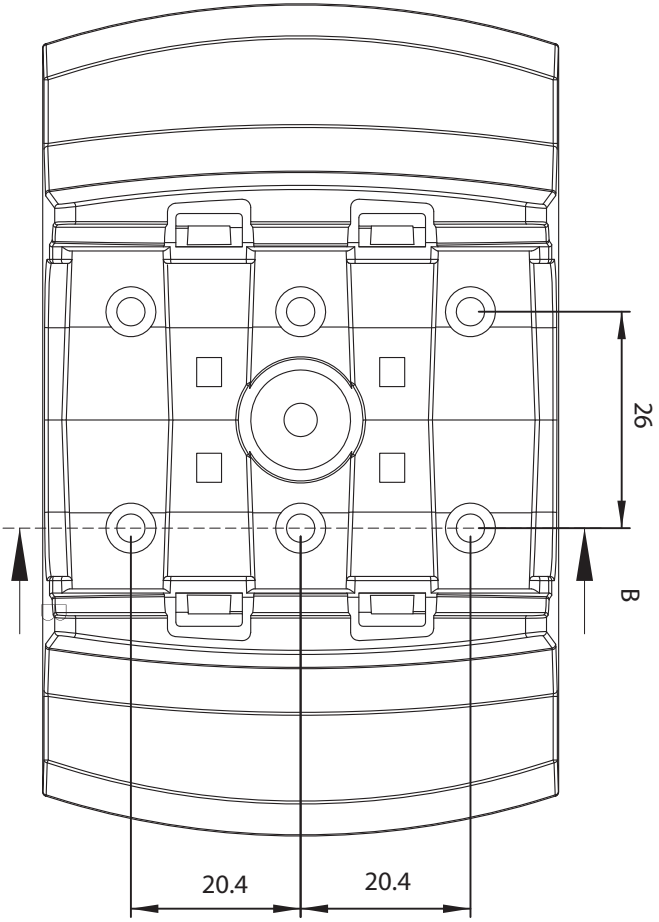

Figure 1-7: Module Stand Top View

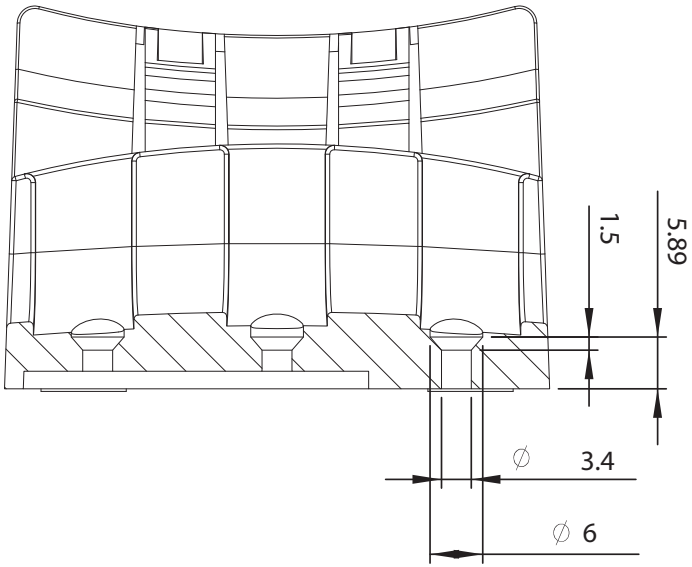

Figure 1-8: Module Stand Side Cutaway View

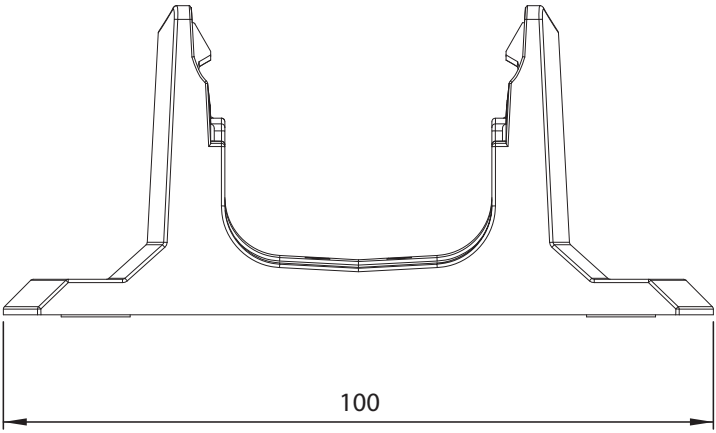

Figure 1-9: Module Stand Front View

1.6 Connector Pin Assignment

The USB-61210 module is equipped with 40-pin removable screw-down terminal connectors, with pin assignment as shown.

	Pin	Pin	
IGND	20	40	IGND
GPI0	19	39	GPO0
GPI1	18	38	GPO1
GPI2	17	37	GPO2
GPI3	16	36	GPO3
GPI4	15	35	IGND
GPI5	14	34	CONV
GPI6	13	33	IGND
GPI7	12	32	AITG
IGND	11	31	NC
IGND	10	30	IGND
AI0-	9	29	AI2-
AI0+	8	28	AI2+
IGND	7	27	IGND
AI1-	6	26	AI3-
AI1+	5	25	AI3+
IGND	4	24	IGND
NC	3	23	NC
NC	2	22	NC
CGND	1	21	IGND

Table 1-1: USB-61210 Pin Assignment

1.6.1 Connector Signal Description

Signal	Reference	I/O	Description
IGND	N/A	None	Isolated ground for AI and DI/O
AI+[0 to 3] AI-[0 to 3]	IGND	I	Differential Input for channels 0 to 3

Signal	Reference	I/O	Description
CGND	N/A	None	Chassis ground
GPI<0..7>	IGND	I	Function Input <0..7> (see Section 3.1.5: Programmable Function I/O)
GPO<0..3>	IGND	O	Function Output <0..3> (see Section 3.1.5: Programmable Function I/O)
CONV	IGND	I	External A/D conversion clock
AITG	IGND	I	Digital trigger for analog input
NC	NC	NC	No connection

Table 1-2: CN1/CN2 I/O Signal Description

1.7 Analog Input Signal Connection

The USB-61210 provides 4 truly differential analog input channels. These four channels are simultaneous-sampling and support up to 2MS/s per channel. The analog signal can be converted to a digital value by the A/D converter. To avoid ground loops and obtain more accurate measurement from the A/D conversion, it is important to understand the type of signal source and how to connect the signal in differential mode.

Signal Source Types

Floating

A floating signal source is not connected in any way to the existing ground system. A device with an isolated output is a floating signal source. This includes optical isolator outputs, transformer outputs, and thermocouples.

Ground-Referenced

A ground-referenced signal is connected in some way to the existing ground system. That is, the signal source is already connected to a common ground point with respect to the USB-61210, assuming that the computer is connected to the same power system. Non-isolated

outputs of instruments and devices that plug into the existing power systems are ground-referenced signal sources.

Input Configurations

Differential Input Mode

Differential input mode provides positive signal and negative signal inputs that respond to signal voltage difference between them, as shown. If the signal source is ground-referenced, differential mode can be used for noise rejection for improvement over single-ended mode.

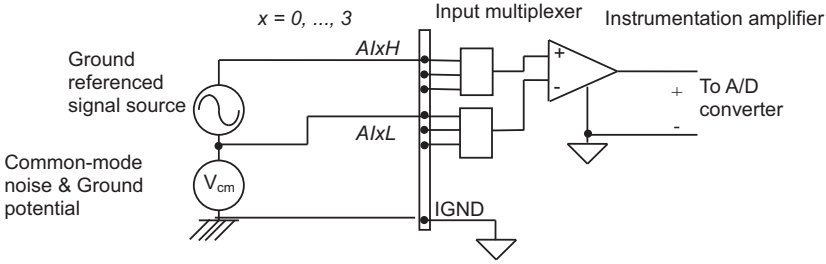

Figure 1-10: GRND-Referenced Source w/ DIFF Input

Connection of a floating signal source to the USB-61210 module in differential input mode is further shown. For floating signal sources, the negative side of the signal should be connected to the AIGND, with less noise coupled into the signal connections than in single-end mode.

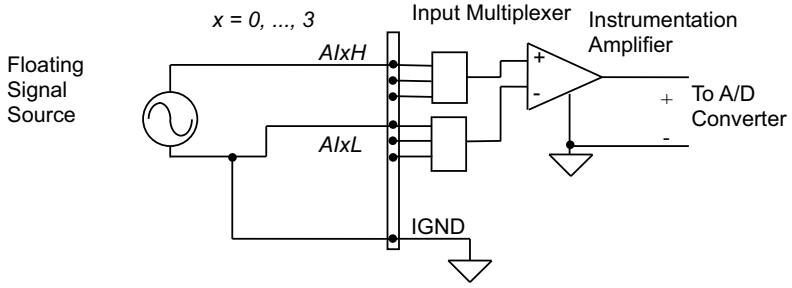

Figure 1-11: Floating Source w/ DIFF Input

1.8 Software Support

JYTEK provides comprehensive software drivers and packages to suit various user approaches to system building. In addition to programming libraries, such as DLLs, for most Windows-based systems, JYTEK also provides drivers for other application environments.

Be sure to install the driver & utility before using the USB-61210 module.

1.9 Driver Support for Windows

UD-DASK

UD-DASK is composed of advanced 32/64-bit kernel drivers and SDK for customized DAQ application development. USB-DASK enables you to perform detailed operations and achieve superior performance and reliability from your data acquisition system. DASK kernel drivers now support Windows 7/8 OS.

1.10 Utilities for Windows

U-Test

U-Test is a free and ready-to-use utility which can assist instant testing and operation of all JYTEK USB DAQ series functions with no programming. In addition to providing data collection and monitoring functions, U-Test also supports basic FFT analysis and provides direct control of analog output and digital I/O with a user-friendly interface.

You can download and install U-Test at: http://www.JYTEK.com/

2 Getting Started

2.1 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to JYTEK. Ensure that the following items are included in the package.

- USB-61210 module
- Stand
- Two removable screw terminals
- USB cable (2-meter length)
- Rail mount kit

2.2 Attaching the Module Stand

The multi-function USB-61210 stand is compatible with desk, rail, or wall mounting. To fix the module in the stand, slide the module body into the stand until a click is heard. To remove the module from the stand, twist the bottom of the stand in a back-and forth motion and separate from the module.

2.3 Rail Mounting

The multi-function stand can be mounted on the DIN rail using the rail-mount kit as shown.

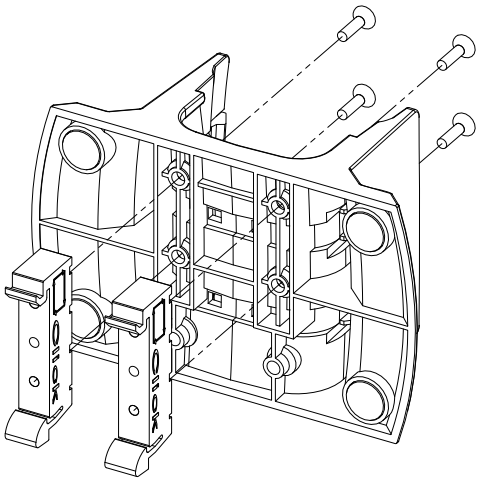

Figure 2-1: Rail Mount Kit

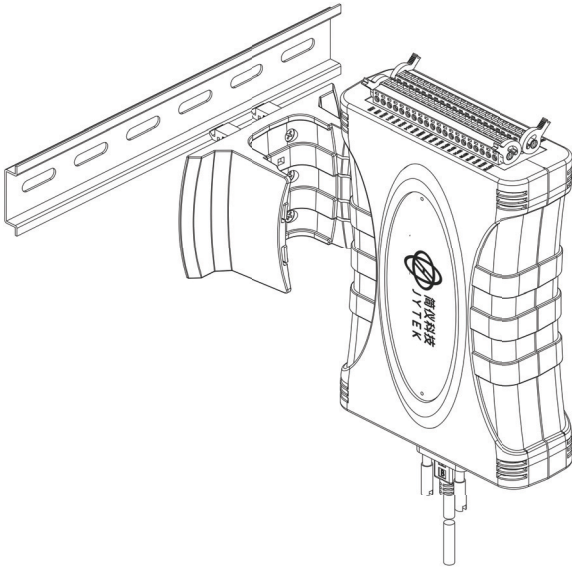

Figure 2-2: Module Pre-Rail Mounting

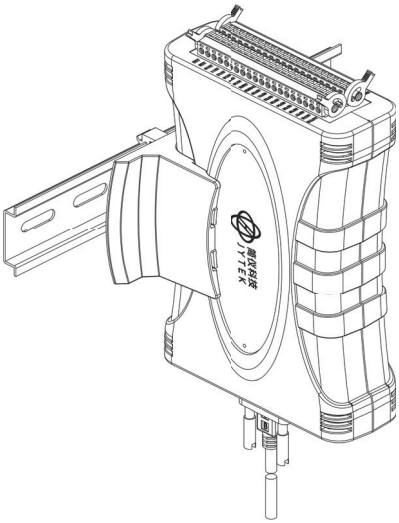

Figure 2-3: Module Rail-Mounted

2.4 Wall Mounting

The multi-function stand can be fixed to a wall using four flush head screws as shown. The four screw holes should be approximately 3.4 mm in diameter.

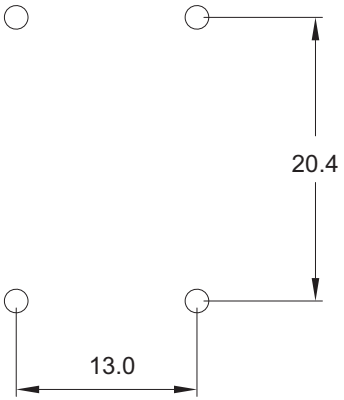

Figure 2-4: Wall Mount Holes

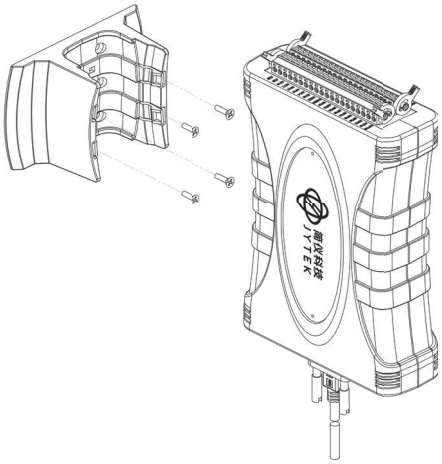

Figure 2-5: Module with Wall Mount Apparatus

2.5 Installing the USB-61210 Module

WARNING:

The appropriate driver must be installed before you can connect the USB DAQ to your computer system. Refer to Section 1.9: Driver Support for Windows for driver support information.

2.5.1 Connecting the USB-61210 Module

1. Turn on your computer.
2. Connect the USB-61210 module to one USB 2.0 port on your computer using the included USB cable.
3. The first time the USB-61210 module is connected, a New Hardware message appears. It will take around 6 seconds to load the firmware. When loading is complete, the LED indicator on the rear of the USB DAQ module changes from amber to green and the New Hardware message closes.
4. The USB-61210 module can now be located in the hardware Device Manager, listed as **JYTEK USBDAQ 61210 Device** as shown.

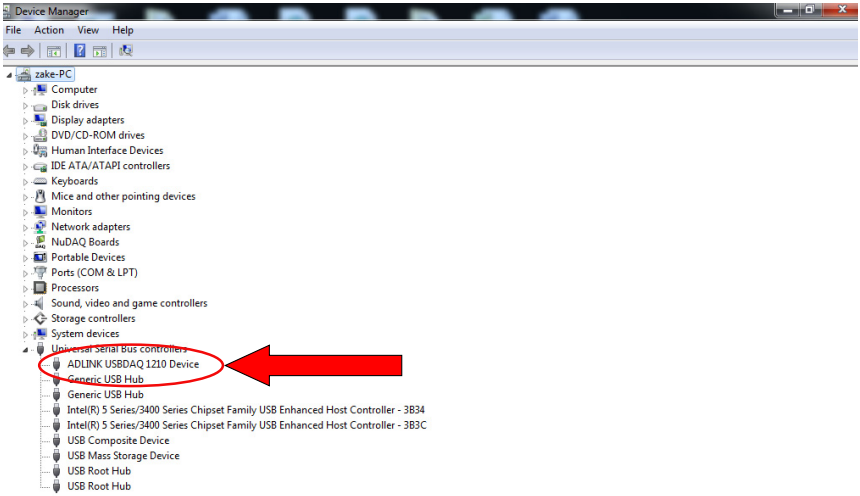

Figure 2-6: USB-61210 module in Windows Device Manager

If the USB-61210 module cannot be detected, the power provided by the USB port may be insufficient. The USB-61210 module is exclusively powered by the USB port and requires 460 mA @ 5 V.

2.5.2 Device ID

A rotary control on the rear of the module (as shown) controls device ID setting and can be set from 1 to 8. The device ID allows dedicated control of the USB-61210 module irrespective of the connected USB port.

When more than one USB module of the same type is connected, each must be set to a different ID to avoid conflicts and errors in operation.

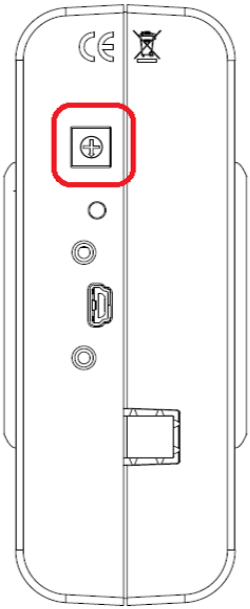

Figure 2-7: Device ID Selection Control

2.5.3 Hardware Configuration

All remaining hardware configurations are software programmable, including sampling/update rate, input/output channel, input range, and others. Please see the UD-DASK Function Reference manual for details.

3 Operation & Calibration

Operation of the USB-61210 is described here to assist in configuration and programming of the module. Functions described include A/D conversion, programmable function I/O, and others

3.1 Operation

3.1.1 Signal Function

The USB-61210 provides 4 truly differential and simultaneous-sampling analog input channels of 16-bit A/D input. Each A/D input channel is connected to one ADC (LT LTC2380 or equivalent). The ADC controller and all timing control logics are implemented by the FPGA. The USB-61210 utilizes calibration circuits to provide high performance and low-temperature drift signal acquisition. Calibration data is saved in the EEPROM.

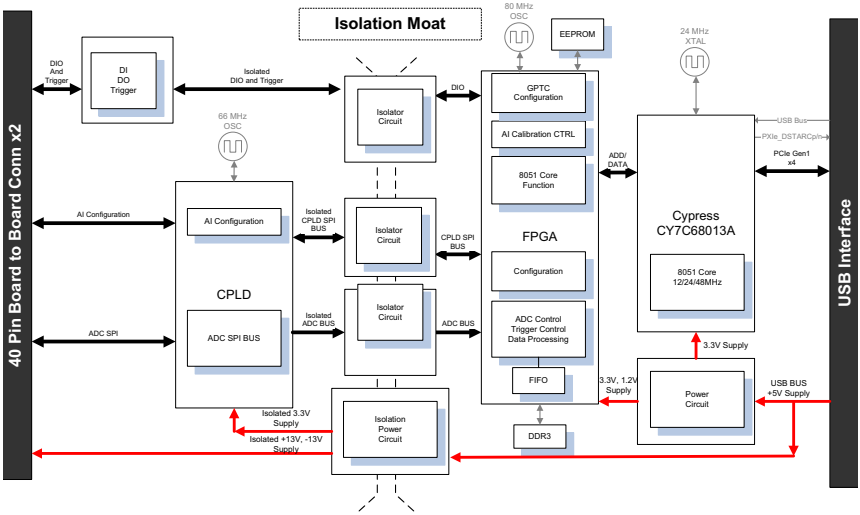

Figure 3-1: Carrier Board Functional Block Diagram

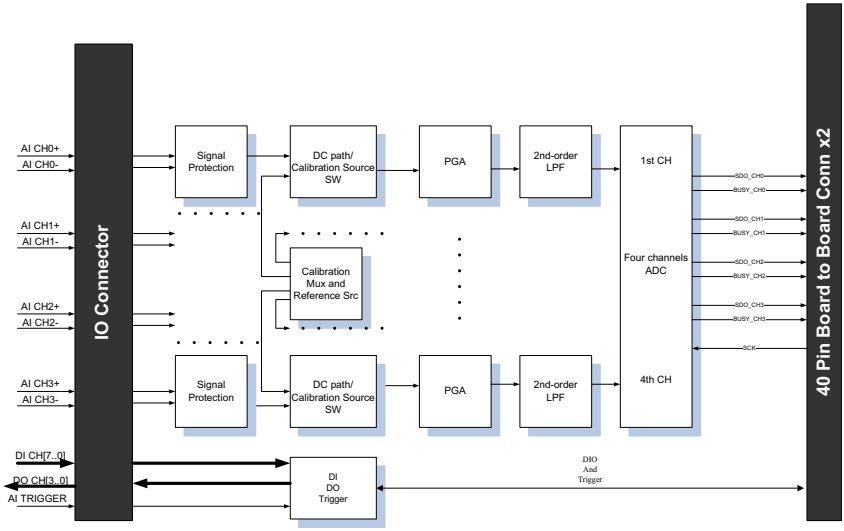

Figure 3-2: Daughter Board Functional Block Diagram

3.1.2 A/D Conversion

When using an A/D converter, the properties of the signal to be measured must be considered and a channel and connection of signals to the module selected. Please see Section 1.7: Analog Input Signal Connection. As well, A/D signal configuration, including channel, gain, and signal type must be defined and set.

A/D acquisition is initiated by a predefined trigger source. Data acquisition will commence once a trigger condition is matched.

After A/D conversion, A/D data is buffered in a data FIFO for transfer into system memory for further processing.

Analog Input Circuitry

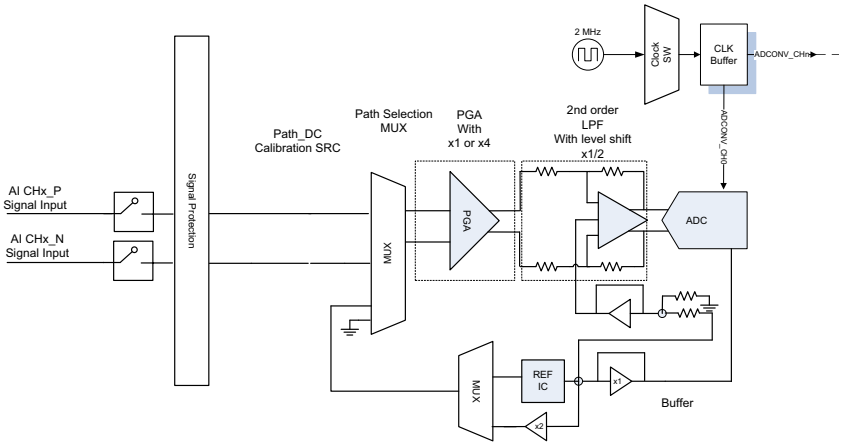

Figure 3-3: Analog Input

AI Data Format

The acquired 16-bit A/D data is 2's complement coded data format. Valid input ranges and ideal transfer characteristics are shown.

Description	Bipolar Analog Input Range		Digital Code
Full-scale range	±10 V	±2 V	N/A
Least significant bit	305.2 µV	61.03 µV	N/A
FSR-1LSB	9.999695V	1.999938V	7FFF
Midscale +1LSB	305.2 µV	61.03 µV	0001
Midscale	0 V	0 V	0000
Midscale –1LSB	-305.2 µV	-61.03 µV	FFFF
-FSR	-10 V	-2 V	8000

Table 3-1: Bipolar Analog Input Range and Output Digital Code

Software Conversion with Polling Data Transfer Acquisition Mode (Software Polling)

Generally the most convenient way to acquire a single A/D data sample, the A/D converter starts a conversion when the dedicated software

command is executed. The software then polls the conversion status and reads back the A/D data when it is available.

This method is indicated when there is a need to process A/D data in real time or instant closed-loop control. In this mode, the timing of the A/D conversion is fully controlled by the software.

WARNING:

The A/D conversion rate is determined by the software timer and may not be precise.

Continuous Acquisition Mode

Continuous A/D Conversion Clock Source

When the onboard ADC receives a conversion clock signal, A/D conversion is triggered. The USB-61210 conversion clock may originate with the internal hardware timer or externally via CONV (external A/D conversion clock) pin. While the conversion clock source can be chosen by setting AI source configuration, if precision acquisition is required, use of the internal hardware timer is recommended.

Sampling Rate Control with Internal Hardware Timer

This mode is recommended if a fixed and precise A/D sampling rate is required.The period between conversions of individual channels can be accurately programmed. ADC sampling rate is determined by:

Sampling Rate = 2M/ScanIntrv Where ScanIntrv is scan interval counter, value can be 1, 2, 3, 4… 2^{32} - 1

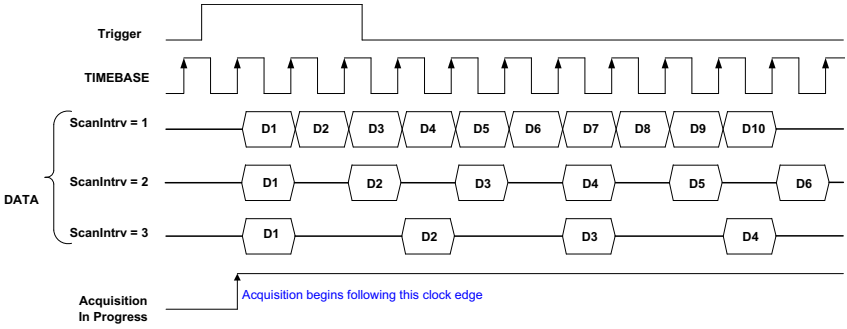

Figure 3-4: Configuring Different Sampling Rates

Sampling Rate Control with External Conversion Strobe Clock

The A/D conversion clock can be provided by external strobe clock via CONV pin. The valid frequency of external clock is from DC to 2 MHz and the minimum pulse width is 225ns.

Analog Input Triggering

The USB-61210 supports flexible trigger sources for analog input functionality. The trigger source can originate with software command, external analog, or external digital signal in continuous analog input mode. Users can configure the trigger source and trigger mode by software.

3.1.3 Trigger Sources

Software Triggering

This trigger mode requires no external trigger source. The trigger asserts immediately following execution of the specified function calls to begin the operation.

External Analog Triggering

The analog multiplexer can select one input channel as the analog trigger source. That is, one of 4 input channels in differential mode can be selected as the analog trigger source. An external analog trigger occurs when the analog trigger signal crosses above (above high) or below (below low) the pre-defined voltage level. The range of trigger level is the full-scale range of the selected input channel and the resolution is 16-bit.

Below-Low Analog Triggering

In below-low analog triggering, as shown, the trigger signal is generated when the input analog signal is less than the Low_Threshold

voltage. High_Threshold setting is not used in this triggering situation.

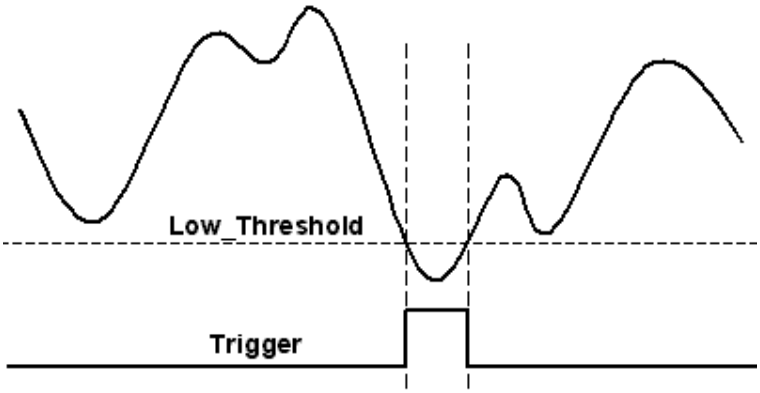

Figure 3-5: Below-Low Analog Triggering

Above-High Analog Triggering

In above-high analog triggering, as shown, the trigger signal is generated when the input analog signal exceeds the High_Threshold voltage. Low_Threshold setting is not used in this triggering situation

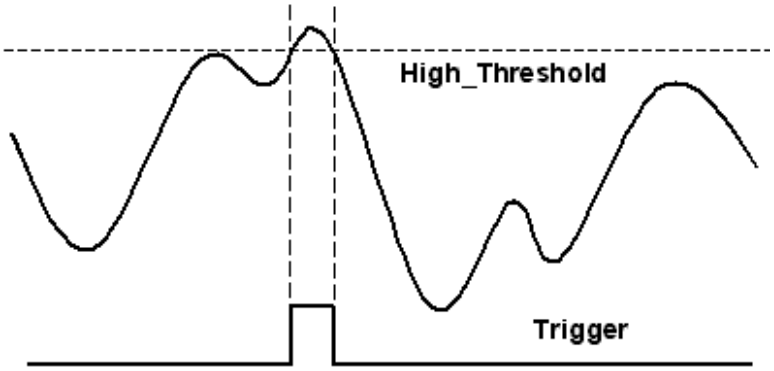

Figure 3-6: Above-High Analog Triggering

External Digital Triggering

An external digital trigger occurs when a rising or falling edge is detected on the digital signal connected to the AITG (analog input trigger) pin. Trigger polarity can be programmed using JYTEK software drivers.

WARNING:

Signal level of the external digital trigger signals should be LVTTL-compatible, with a minimum pulse of 20ns.

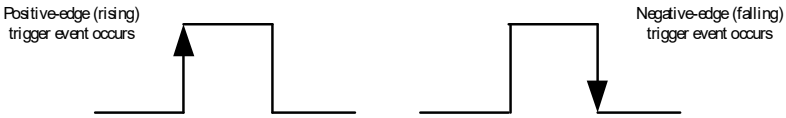

Figure 3-7: Digital Triggering

3.1.4 Trigger Modes

Analog input supports post, pre, middle, delay, gate, post trigger with retrigger, and delay trigger with retrigger modes.

Post-Trigger Acquisition Mode (no retriggering)

Post-trigger acquisition is indicated when data is to be collected after the trigger event, as shown..

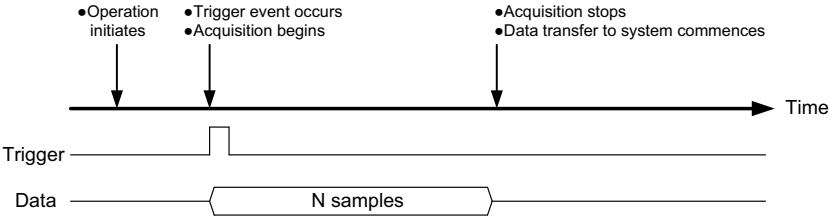

Figure 3-8: Post Trigger without Retriggering

Delayed-Trigger Acquisition Mode (no retriggering)

Delay-trigger acquisition is indicated when the data collection is to be delayed following the trigger event, as shown. Delay duration is specified by a 32-bit counter value, whereby maximum delay is the period of TIMEBASE X (2^{32} - 1), and minimum delay the period of the timebase.

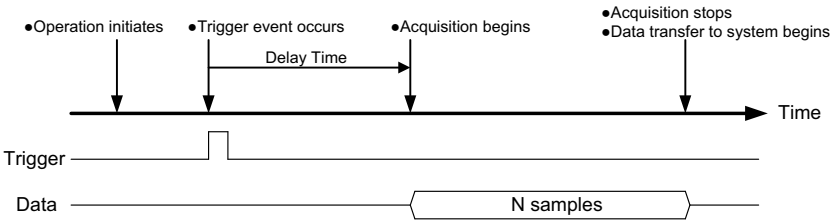

Figure 3-9: Delayed Trigger

Middle Trigger Mode

Middle-trigger acquisition mode is indicated when data is to be collected before and after the trigger event. The amount of stored data before and after trigger event can be set individually (M and N samples), as shown.

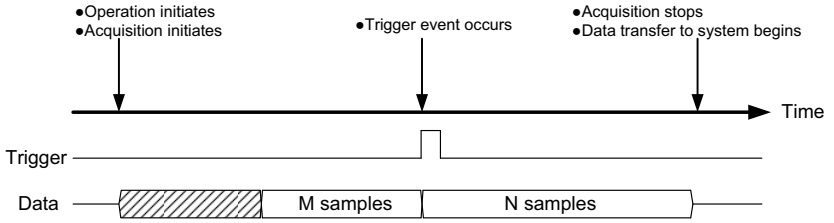

Figure 3-10: Middle Trigger

Pre-Trigger Mode

Pre-trigger acquisition is indicated when data is to be collected before the trigger event. Acquisition commences once specified function calls are executed to begin the pre-trigger operation, and stops when the trigger event occurs. If the trigger event occurs after the specified amount of data has been acquired, the system stores only data preceding the trigger event by a specified amount, as shown.

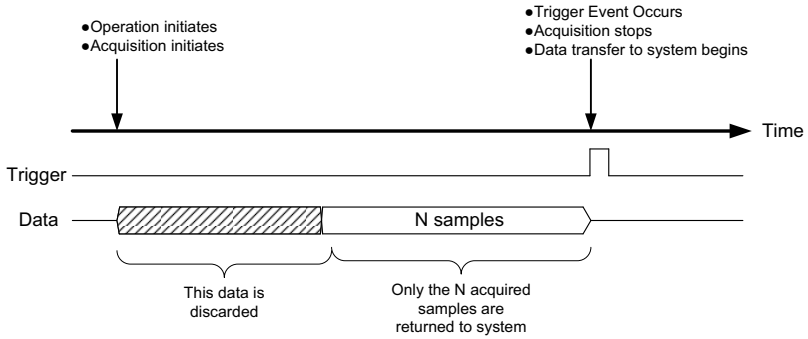

Figure 3-11: Pre-Trigger

Post-Trigger or Delayed-Trigger Acquisition Mode with Retriggering

Post-trigger or Delayed-Trigger acquisition with re-trigger function is indicated when data is to be collected after several trigger events. An example is shown, in which N samples of data are acquired after the first trigger signal, after which the USB-61210 awaits the next re-trigger signal (re-trigger signals occurring before the N samples are completed will be ignored). When the re-trigger signal occurs, another N samples are performed. The process repeats until the specified number of re-trigger signals are detected.

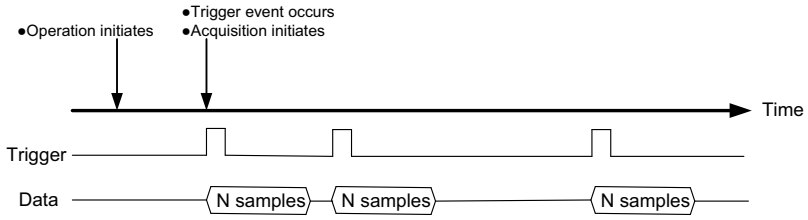

Figure 3-12: Post Trigger with Retriggering

Gated Trigger

Gated-trigger acquisition is indicated in applications where you want to collect data when trigger events are set to level high/low, and hold acquisition when trigger events are set to the opposite level.

As shown, after the operation starts, the first scan of data is immediately acquired when the trigger signal is deasserted and paused when the trigger signal is asserted.

The remaining A/D conversions are not performed until the trigger signal is deasserted again. The process repeats until the specified amount of data is acquired.

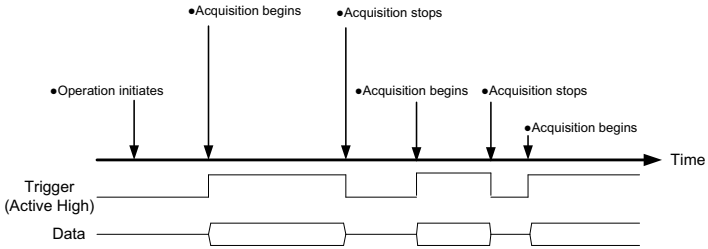

Figure 3-13: Gated Trigger

3.1.5 Programmable Function I/O

The USB-61210 supports powerful programmable I/O function provided by an FPGA chip, configurable as LVTTL DI/DO, 32-bit timer/counters, and PWM output. These signals are single-ended and 5 V LVTTL-compliant.

LVTTL DI/DO

Programmable function I/O can be used as static LVTTL-compliant 8-CH digital input and 4-CH digital output. You can read/write these I/O lines by software polling, with sample and update rate fully controlled by software timing.

	Pin#	Pin#	
IGND	20	40	IGND
GPI0	19	39	GPO0
GPI1	18	38	GPO1
GPI2	17	37	GPO2
GPI3	16	36	GPO3

	Pin#	Pin#	
GPI4	15	35	IGND
GPI5	14	34	N/C*
GPI6	13	33	N/C*
GPI7	12	32	N/C*
IGND	11	31	N/C*

*Not used in DI/O

Table 3-2: Pin Definition of LVTTL Digital I/O

General Purpose Timer/Counter

The USB-61210 is equipped with two general purpose timer/counter sets featuring:

- Count up/down controllable by hardware or software
- Programmable counter clock source (internal clock up to 80 MHz, external clock up to 10 MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial Count loaded from a software application
- Current count value readable by software without affecting circuit operation.

	Pin	Pin	
IGND	20	40	IGND
GPTC_CLK	19	39	GPTC_OUT0
GPTC_UD0	18	38	GPTC_OUT1
GPTC_GATE0	17	37	GPTC_OUT2
GPTC_AUX0	16	36	GPTC_OUT3
GPTC_CLK2	15	35	IGND
GPTC_UD2	14	34	N/C*
GPTC_GATE2	13	33	N/C*
GPTC_AUX2	12	32	N/C*

	Pin	Pin	
IGND	11	31	N/C*

*Not used in GPTC

Table 3-3: Timer/Counter Pin Definition

3.1.6 Basic Timer/Counter Function

Each timer/counter has three inputs that can be controlled via hardware or software. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UD). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input increment or decrement the counter. The GPTC_UD input directs the counter to count up or down (high: count up; low: count down), while the GPTC_GATE input is a control signal acting as a counter enable or counter trigger signal in different applications. The GPTC_OUT then generates a pulse signal based on the timer/counter mode set.

All input/output signal polarities can be programmed by software application. For brevity, all GPTC_CLK, GPTC_GATE, and GPTC_OUT in the following illustrations are assumed to be active high or rising-edge triggered.

3.1.7 General Purpose Timer/Counter Modes

Ten programmable timer/counter modes are available. All modes initialize following a software-start signal set by the software. The GPTC software reset initializes the status of the counter and reloads the initial value to the counter. The operation remains halted until software start is executed again. Operations under different modes are described as follows.

Mode 1: Simple Gated-Event Counting

In this mode, the counter calculates the number of pulses on the GPTC_CLK after a software start. Initial count can be loaded from the software application. Current count value can be read back by software any time with no influence on calculation. GPTC_GATE enables/disables calculation. When GPTC_GATE is inactive, the counter halts the current count value. Operation in which initial count = 5, countdown mode is shown.

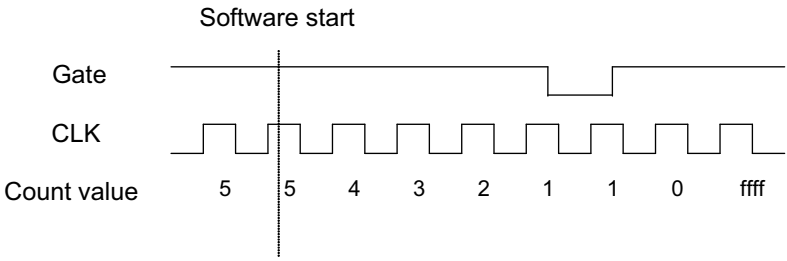

Figure 3-14: Mode 1-Simple Gated-Event Calculation

Mode 2: Single Period Measurement

The counter calculates the period of the signal on GPTC_GATE in terms of GPTC_CLK. The initial count can be loaded from the software application. After software start, the counter calculates the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the completion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read by the software application. Operation in which initial count = 0, count-up mode is shown.

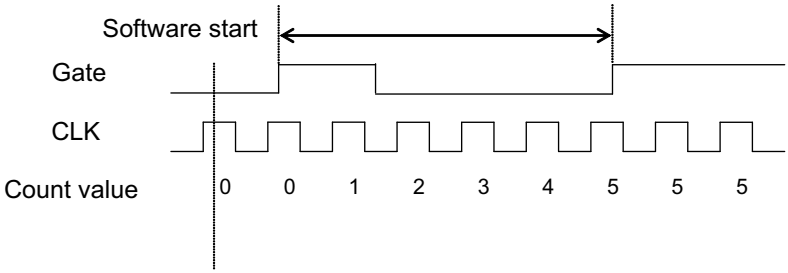

Figure 3-15: Mode 2-Single Period Measurement

Mode 3: Single Pulse-Width Measurement

The counter calculates the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from the software appli-

cation. After software start, the counter calculates the number of active edges on GPTC_CLK when GPTC_GATE is in its active state.

After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high and current count value can be read by the software application. Operation in which initial count = 0, count-up mode is shown.

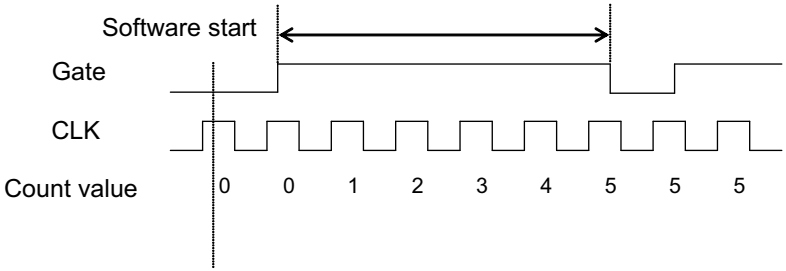

Figure 3-16: Mode 3-Single Pulse-Width Measurement

Mode 4: Single-Gated Pulse Generation

This mode generates a single pulse with programmable delay and programmable pulse-width following software start. The two programmable parameters can be specified in terms of periods of the GPTC_CLK input by the software application. GPTC_GATE enables/disables calculation. When GPTC_GATE is inactive, the counter halts the current count value. Generation of a single pulse with a pulse delay of two and a pulse-width of four is shown.

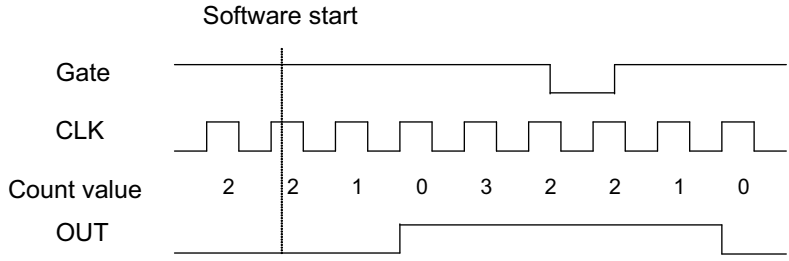

Figure 3-17: Mode 4-Single-Gated Pulse

Mode 5: Single-Triggered Pulse

This mode generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. These programmable parameters can be specified in terms of periods of the GPTC_CLK input. When the first GPTC_GATE edge triggers the single pulse, GPTC_GATE has no effect until software start is executed again. Generation of a single pulse with a pulse delay of two and a pulse-width of four is shown.

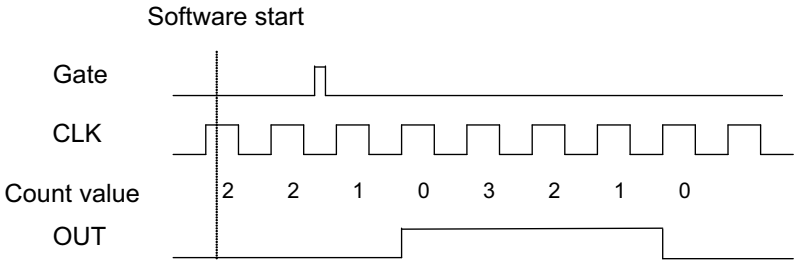

Figure 3-18: Mode 5-Single-Triggered Pulse

Mode 6: Re-Triggered Single Pulse Generation

This mode is similar to Mode 5 except that the counter generates a pulse following every active edge of GPTC_GATE. After software start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse width. Any GPTC_GATE triggers that occur when the prior pulse is not completed are ignored. Generation of two pulses with a pulse delay of two and a pulse width of four is shown.

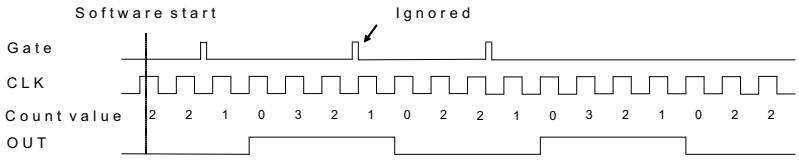

Figure 3-19: Mode 6-Re-Triggered Single Pulse

Mode 7: Single-Triggered Continuous Pulse Generation

This mode is similar to Mode 5 except that the counter generates continuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. When the first GPTC_GATE edge triggers the counter, GPTC_GATE has no effect until software start is executed again. Generation of two pulses with a pulse delay of four and a pulse-width of three is shown.

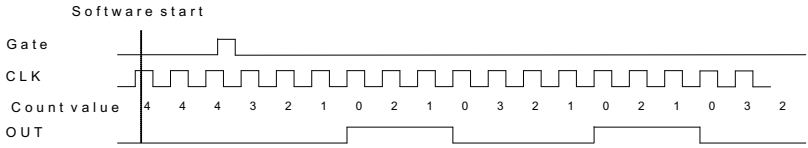

Figure 3-20: Mode 7-Single-Triggered Continuous Pulse

Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following software start. GPTC_GATE enables/disables calculation. When GPTC_GATE is inactive, the counter halts the current count value. Generation of two pulses with a pulse delay of four and a pulse-width of three is shown.

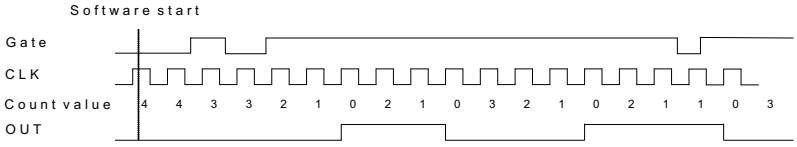

Figure 3-21: Mode 8-Continuous Gated Pulse

Mode 9: Edge Separation Measurement

Measures the time differentiation between two different pulse signals. The first pulse signal is connected to GPTC_GATE and the second signal is connected to GPTC_AUX. Clocks that pass between the rising edge signal of two different pulses through the 80 MHz internal clock or external clock are calculated. You can calculate the time period via the known clock frequency. The maximum counting width is 32-bit.

Decrease of the counter value in Edge Separation Measurement mode is shown.

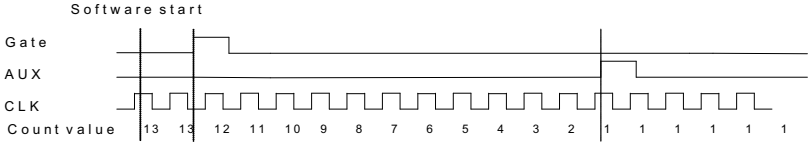

Figure 3-22: Mode 9-Edge Separation Measurement

Mode 10: PWM Output

The USB-61210 timer/counter can also simulate a PWM (Pulse Width Modulation) output. The PWM starts to generate output following a GPTC_GATE edge trigger or being activated/inactivated by the GPTC_GATE high/low logic control. By setting a varying amount of Pulse_initial_cnt and Pulse_length_cnt, varying pulse frequencies (Fpwm) and duty cycles (Dutypwm) can be obtained. PWM output is shown.

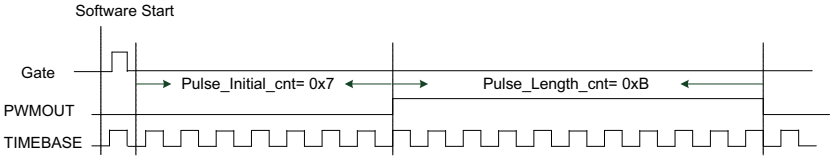

Figure 3-23: Mode 10-PWM Output Following Trigger

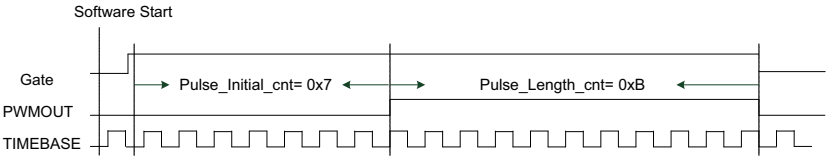

Figure 3-24: Mode 10-PWM Output Following GATE Control

Calculation of the PWM frequency and duty cycle is as follows.

$$F_{PWM} = \frac{F_{Timebase}}{Pulse\_initial\_cnt + Pulse\_length\_cnt}$$

$$Duty_{PWM} = \frac{Pulse\_length\_cnt}{Pulse\_initial\_cnt + Pulse\_length\_cnt}$$

3.1.8 Isolation

The USB-61210 provides 500VDC isolation capability to protect against hazardous voltage caused by erroneous signal connection or signal levels to be measured exceeding expectation. The isolation circuit can also reduce the ground-loop noise.

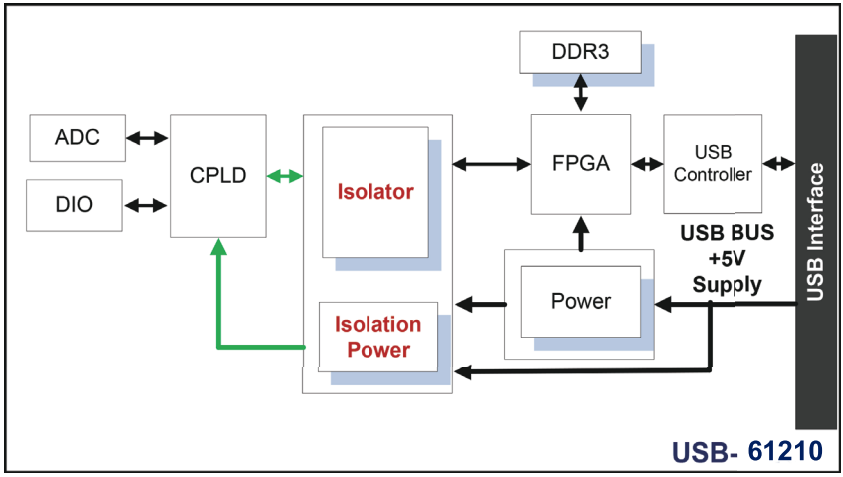

Figure 3-25: Isolation

3.2 Calibration

3.2.1 Loading Calibration Constants

The USB-61210 is factory-calibrated before shipment. The associated calibration constants of the TrimDACs firmware are written to the onboard EEPROM. TrimDACs firmware is the algorithm in the FPGA.

Loading calibration constants entails loading the values of TrimDACs firmware stored in the onboard EEPROM.

Dedicated space for storing calibration constants is provided in the EEPROM. In addition to the bank of factory calibration constants, there is one user-utilization bank, allowing loading of the TrimDACs firmware values either from the original factory calibration or a subsequently-performed calibration.

The default calibration constants are loaded from the user-utilization bank and are the same as those in the factory calibration bank if no auto-calibration is performed.

Since measurement and output errors may vary depending on time and temperature, it is recommended that you calibrate the USB-61210 module in your existing testing environment, as follows.

3.2.2 Auto-Calibration

USB-61210 auto-calibration utility measures and corrects almost all calibration errors with no external signal connections, reference voltage, or measurement devices. The USB-61210 provides onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured in the production line by a digital potentiometer and compensated in the software. The calibration constant is stored after this measurement.

3.2.3 Saving Calibration Constants

Factory-calibrated constants are permanently stored in a bank of the onboard EEPROM and cannot be modified. When the device is recalibrated, the software stores the new constants in a user-configurable section of the EEPROM. To restore original factory calibration settings, the software can copy the factory-calibrated constants to the user-configurable section of the EEPROM. When auto-calibration is complete, the new calibration constants can be saved to the user-configurable banks in the EEPROM.

NOTE:

The USB-61210 should be warmed up for at least 15 minutes before initiating auto-calibration

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Warranty Policy

Thank you for choosing JYTEK. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. All JYTEK products come with a limited two-year warranty:
   - ▷ The warranty period starts on the day the product is shipped from JYTEK's factory.
   - ▷ Peripherals and third-party products not manufactured by JYTEK will be covered by the original manufacturers' warranty.
   - ▷ For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. JYTEK is not responsible for any loss of data.
   - ▷ Please ensure the use of properly licensed software with our systems. JYTEK does not condone the use of pirated software and will not service systems using such software. JYTEK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - ▷ For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. JYTEK is not responsible for items not listed on the RMA Request & Confirmation Form.

2. Our repair service is not covered by JYTEK's guarantee in the following situations:
   - ▷ Damage caused by not following instructions in the User's Manual.
   - ▷ Damage caused by carelessness on the user's part during product transportation.
   - ▷ Damage caused by fire, earthquakes, floods, lightening, pollution, other acts of God, and/or incorrect usage of voltage transformers.
   - ▷ Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - ▷ Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - ▷ Damage from improper repair by unauthorized JYTEK technicians.
   - ▷ Products with altered and/or damaged serial numbers are not entitled to our service.
   - ▷ This warranty is not transferable or extendible.
   - ▷ Other categories not protected under our warranty.
3. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

If you have any further questions, please email our service center: service@jytek.com.

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